SELF-ALIGNED TRENCH ISOLATION METHOD AND SEMICONDUCTOR DEVICE FABRICATED USING THE SAME

ABSTRACT OF THE DISCLOSURE

A method according to some embodiments of the invention includes forming a first gate pattern on a first region of a semiconductor substrate. The first gate pattern is formed to have a first gate insulating layer pattern, a first lower gate conductive layer pattern and a gate etching stopper layer pattern which are sequentially stacked. A second gate pattern is formed on a second region spaced apart from the first region to define a border region between the first and second regions. The second gate pattern is formed to have a second gate insulating layer pattern and a second lower gate conductive layer pattern, which are sequentially stacked. Thus, some embodiments may prevent two different gate conductive layers from overlapping with each other in the border region. Accordingly, semiconductor memory devices according to some embodiments of the invention do not have undesired active regions formed in the border region.